IFW

TAM-103

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Appl. No.	:	10/531,287	Confirmation No. 4868
Applicant	:	T. TANIMOTO et al	
Filed	:	April 14, 2005	
Title	:	COMPILER AND LOGIC CIRCUIT DESIGN METHOD	
TC/AU	:	2825	
Examiner	:	S. Parihar	
Docket No.	:	TAM-103	
Customer No.:		24956	

INFORMATION DISCLOSURE STATEMENT
UNDER 37 CFR 1.97 & 1.98

Commissioner for Patents
Mail Stop DD
P.O. Box 1450
Alexandria, VA 22313-1450

Sir:

In accordance with the duty of disclosure, the Applicants submit the documents cited on the attached PTO-1449 form.

The non-patent literature documents listed in the attached PTO-1449 form were previously submitted with an Information Disclosure Statement on April 14, 2005. However, the Examiner has requested additional date information and document copies. The information has been added and reentered on a new PTO-1449 Form, and the requested copies are attached.

Date information has been added to references AP and AQ.

In the PTO-1449 form filed on April 14, 2005, the Nikkei Electronics reference was incorrectly entered as two references, namely AT and AU. This has been corrected and entered as reference AU on the attached PTO-1449 Form, and a copy of said reference is

attached.

A copy of the AV reference is enclosed.

No explanation of relevancy is being provided for the documents because each is either in the English language, discussed in the present Specification, or its relevance is as stated in a communication from a foreign patent office in a counterpart foreign application.

The Applicants request the Examiner initial and return a copy of the attached PTO-1449 form as an indication that the references have been considered.

If a fee or additional fee is required, the Commissioner is hereby authorized to charge any fee or additional fee that may be required and credit any excess to Deposit Account No. 50-1417.

Respectfully submitted,

Mattingly, Stanger, Malur & Brundidge, P.C.

John R. Mattingly
Registration No. 30,293
Telephone: (703) 684-1120

Date: April 5, 2007

Form PTO-1449	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DKT. NO.	SERIAL NO.
		TAM-103	10/531,287
INFORMATION DISCLOSURE STATEMENT BY APPLICANT (Use several sheets if necessary)		APPLICANT: T. TANIMOTO, et al.	
		FILING DATE: April 14, 2005	GROUP: 2825

U.S. PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Name	Class	Subclass	Filing Date
	AA						
	AB						
	AC						
	AD						
	AE						
	AF						
	AG						
	AH						
	AI						
	AJ						
	AK						
	AL						

FOREIGN PATENT DOCUMENTS

Examiner Initial		Document Number	Date	Country	Class	Subclass	Abstract	
							Yes	No
	AM							
	AN							
	AO							
	AP							
	AQ							
	AR							
	AS							
	AT							

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

	AP	C-based Synthesis Experiences with a Behavior Synthesizer, "Cyber" Wakabayashi, et al., 1999.
	AQ	IEEE Std 1076, 2000 Edition. IEEE Standard VHDL Language Reference Manual, December 29, 2000.
	AR	
	AS	
	AT	
	AU	Kazutoshi Wakabayashi et al., "Densoyo LSI o Dosa"Gosei de Kaihatsu, Kino Sekkei no Kikan ga 1/10 ni Tanshuku", Nikkei Electronics, Nikkei Business Publications, Inc., 12 February , 1996 (12.02.96), No. 6555, pages 147-169.
	AV	Kurokawa, H. et al., "C++ Based System Simulator for Pre-Verification of System-on-a-Chip Devices", NEC Research & Development, 07 December, 2000 (07.12.00), Vol. 41, No.3, pages 258-263.

Examiner	Date Considered